

**REMARKS**

Claims 1-44 remain pending in the current Application. Claims 1 and 30 have been amended. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claims 1-44 have been rejected under 35 U.S.C. 112. Applicants wish to thank the Examiner for the phone interview on June 17, 2008, to clarify the 112 issues. Applicants explained how a single instruction can specify a size of data element in memory separate and independent from a size of data element in at least one general purpose register, and pointed to the Ivex instruction of FIG. 2 as an example. As a result of the conversation, Applicants have amended claims 1 and 30, as suggested by the Examiner, in order to further clarify the claims and not for patentability reasons. Therefore, claims 1 and 30 include “wherein the size of data elements in memory, specified by the first single instruction, is separate and independent from the size of data elements in the at least one general purpose register, specified by the first single instruction.” There are many instructions described in the specification that provide support for specifying the size of data elements in memory separate and independent from the size of data elements in the at least one general purpose register. For example, see the vector load instructions of FIGs. 2-7, 27, 28, and 31 which each include the ability to specify the size of data elements in memory (“ms”) separate and independent from the size of data elements in the destination register (“ds”) and the vector store instructions of FIGs. 8-11 and 32 which each include the ability to specify the size of data elements in source register (“ss”) separate and independent from the size of data elements in memory (“ms”). Since the size of data elements in memory is separate and independent from the size of data elements in the at least one general purpose register, the sizes can be the same or different. See, for example, page 12, lines 1-18. See also the example Ivex instructions on page 32 which use the same size, e.g. a halfword data element size in memory (“mh”) and a halfword data element size in the destination register (“dh”), and the example Ivex instruction on page 38 which uses different sizes, e.g. a byte data element size in memory (“mb”) but a halfword data element size in the

destination register ("dh"). Therefore, for at least these reasons, Applicants submit that claims 1 and 30 are patentable under 35 U.S.C. 112.

Claims 2-29 and 31-44 have not been independently addressed since they depend directly or indirectly from allowable claim 1 or 30 are therefore allowable for at least those reasons which apply to claims 1 and 30.

### **Conclusion**

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

#### **SEND CORRESPONDENCE TO:**

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